TECHNOLOGICAL UNIVERSITY OF THE PHILIPPINES

ELECTRONICS ENGINEERING DEPARTMENT

**ASSIGNMENT NO**. 1

CPET11 – BET-CPET-3A / 7:00 AM – 10:00 AM W

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As a group, work on the following requirements (only group leaders will upload/turn in):  
  
**1.     Explain in layman’s terms (1 paragraph or 5 sentences max) the microprocessor operation as shown in Table 2. (25 points)**

The microprocessor works like a smart calculator that follows a step-by-step process to handle data, such as solving 1 + 3 = 4. When a key is pressed, the Bus Unit receives the instruction, the Pre-fetch Unit confirms it, stores the code in the Instruction Cache, and then forwards it to the Decode Unit, which converts the human-readable command into binary machine code for the Control Unit. The Control Unit stores numbers like 1 and 3 in the Data Cache and waits for the '+' command, after which it instructs the Arithmetic Logic Unit (ALU) to perform the addition and store the result in a register address. Once the equal sign is pressed, the instruction again goes through the fetch-decode process, and the Control Unit fetches the stored result from the register. Finally, the result is sent through the Bus Unit to the output display, showing the correct answer of 4.

**2.     If you were to design a microcomputer system, which architecture (i.e., Von Neumann or Harvard) will you use and why? Enumerate at least 5 advantages and disadvantages of each. (25 points)**

If our group wants to design a microcomputer system, we will be using the Harvard architecture because it is faster, efficient, and secure unlike the Von Neumann architecture. Since Harvard uses separate memories and buses, the CPU can fetch data simultaneously that can lead to faster outputs. The Harvard architecture is also reliable for real time embedded systems which can be beneficial for our course especially in our thesis, where we are required to incorporate IoT and robotics which speed and accuracy are important. Although it is more expensive and needs complex designing, it is a better choice for our group because of more powerful performance and can be on par and keep up with modern technologies nowadays.

**Advantages and Disadvantages**

       In Module 1 - Introduction to Microprocessors and Microcontroller, our group learned the two main types of microprocessor architecture naming the Von Neumann architecture and Harvard architecture. Von Neumann architecture is designed where both your instructions and data are stored in the same memory space and accessed only through a single pathway. On the other hand, Harvard architecture uses separate memories and buses for data and instructions. So, because of these designs, we have come up with each of the architecture’s advantages and disadvantages with the help of researching through the internet.

Advantages of Von Neumann architecture:

1. Simple design because of using only single memory design and no need for complicated routing.
2. Low cost because of small number of components and memory chips required
3. It is flexible because you can easily modify the program since data and instructions are stored together.
4. Memory efficient because there is no need to separate storage for data and instructions
5. It is very common architecture that most general computers use this setup

Disadvantages of Von Neumann architecture:

1. There is a bottleneck issue because the CPU can only get instructions and data one at a time.
2. Because of the bottleneck mentioned above, it has slow speed and performance
3. The program is less secure since the instructions and data are mixed in a single memory space.
4. Not for high performance systems and real time tasks
5. Consumes more power because instructions and data share the same bus that makes latency and less efficient

Advantages of Harvard architecture:

1. It is faster because it can fetch data and instructions at the same time
2. No bottleneck because of separate pathways that means less waiting time for the memory
3. More secure because instructions and data are separate, so they don’t overwrite each other
4. Harvard architecture is more power efficient
5. It is good for embedded systems and real time tasks.

Disadvantages of Harvard architecture:

1. It needs more planning and complex design
2. It is more expensive because it consists of more memories and bus routing.
3. Harder for programs to modify because of separated instruction and data memory
4. Waste of memory because sometimes data memory is full, but the instruction memory is empty or vice versa.
5. Harder to design and control because timing and bus management is trickier.

**3.     Design a sample IPO system using a microprocessor or microcontroller. Identify the parts and specify the main function of the system. (25 points)**

**Thermistor Heat Detection System**

**OUTPUT**

If the certain range or condition is met, a buzzer and an LED will activate to give an “alarm” that it is too hot.

**PROCESS**

The Arduino Uno will act as a brain to decode the given data by the Thermistor and will compare it to a preset threshold to display if a certain range or condition is reached.

**INPUT**

With the use of the Thermistor, it will function as a sensor to detect the temperature of the surroundings and will change its resistance depending on how hot it is.

|  |  |
| --- | --- |
| **PARTS** | **FUNCTIONS** |
| Thermistors Basics THERMISTOR | It acts as the input sensor wherein its resistance changes proportional to its temperature, allowing Arduino to interpret the data. |
| Arduino - Wikipedia  ARDUINO UNO | The brain of the system, it will process the data and will decide when to activate the alarm. |
| 1k Ohm Resistor  10KΩ RESISTOR | Works with the thermistor and acts as a voltage divider in order to convert it into a measurable voltage |
| 4110-40, 200mm Jumper Wire Breadboard Jumper Wire in Black, Blue, Brown,  Green, Grey, Orange, Purple, Red, White, Yellow  JUMP WIRES | Provides connections for all the parts to come together. |
| 5V Active Electromagnetic Buzzer  BUZZER | The buzzer will become the alert system by producing a sound if the Arduino activates it. |
| Lite-On2.6 V Red LED 5mm Through Hole, LTL-307P  LED | The LED will become the alert system by producing a light if the Arduino activates it. |
| Power supply - Wikipedia  POWER SOURCE | For the system to work we need power. |

**Main Function**

The *Thermistor Heat Detection System* is designed to continuously detect anomalies in the temperature specifically if it’s getting too high and will continue to alarm until the temperature subsides. The thermistor will act as the sensor, changing its resistance with temperature. Afterwards, it will then get decoded by the brain or the Arduino. Finally, releasing an alarm through buzzer and LED. It can help places that need specific temperature only for example in a medicine store, there are certain drugs or medicine that needs to be kept in a certain temperature, by this system they can prevent from the medicine getting damaged.

**4.     Research on at least 5 trends in microprocessors or microcontrollers. Specify the key proponent/s, timeline, and applications. Provide data in terms of figures and tables. Cite at least 5 references using APA v7. (25 points)**

1. **INTEGRATION OF AI/MACHINE LEARNING ON MICROPROCESSORS**

With the current trend with regards to Artificial Intelligence (AI) and Machine Learning, modern microprocessors as well as Microcontroller Units (MCU) have utilized the aforementioned technology in order to accelerate computing time and accomplish more processes quicker. By default, processors are able to accomplish processes “serially.” The utilization of “context-switching” (a processor technique utilized in order to efficiently change processes according to a process’ criticality while saving the state of a previous process) makes it seem that processors are multi-tasking threads and processes where in reality, it is actually the opposite. Through the integration of AI technology and Machine Learning on modern processors (as well as graphics processing units), actual parallelism and enhance pipelining is achieved.

The first proponent of artificial intelligence would be Alan Turing. On his paper entitled, “Computing Machinery and Intelligence” which was published in the year 1950, Alan Turing formulated the “Turing test” of which determines if a machine has the capacity to think on its own. In 1956, John McCarthy held a conference in Dartmouth College in New Hampshire, USA. The conference is now considered the actual founding of the term Artificial Intelligence (AI). He discussed how machines can learn to use abstract languages such as machine code and even natural language while aiding humans in the process to simplify significant tasks (Lawrence Livermore National Library, n.d.). Years after the formal definition of AI, numerous individuals have formulated AI technology in either emulating human decisions or utilizing rapid decision making to accelerate process accomplishment. A dissertation from James Robert Slagle further pushed the industry. His dissertation entitled, “A Heuristic Program that Solves Symbolic Integration Problems in Freshman Calculus” introduces SAINT. SAINT or Symbolic Automatic Integrator was a heuristic program that Slagle formulated in order to emulate the decision-making of a freshman student in solving integral calculus problems (AIWS, 2025).

After SAINT, research on Artificial Intelligence slowed down. However, the 1990’s and onwards presented an uptrend in AI research and development with more emphasis on data-heavy and specific issues instead of human emulation (Lawrence Livermore National Library, n.d.). This applies to modern microprocessors that utilizes AI to accelerate its computing power. The development of AI can be directly correlated to the rapid innovation of microprocessors. By this time, multiple AI models have been formulated for specific tasks or accelerating output. Despite the commendable sequential speed of microprocessors during the 2010’s, it could only improve performance up to a certain extent. The aforementioned AI models were to taxing to run and required much computational power in order to be ran properly in real time (Khan, Pasha, & Masud, 2021). In response to this, microprocessor companies have embedded deep learning algorithms and hardware on their microchips in order to combat this bottleneck. Intel formulated the Math Kernel Library and integrated “Intel Deep Learning Boost Library” on their processors for improved real time performance for AI models. Through Intel DL Boost Library, various AI models for speech recognition, object detection and other AI model specific tasks were vastly improved (Khan, Pasha, & Masud, 2021).

Executing AI models are parallel in nature. No matter the implementation of deep learning and machine learning on microprocessors, its sequential nature would never reach to levels of which it could be considered efficient. Graphics Processing Units run in parallel at its core. NVDIA took advantage of this fact and developed a library entitled “Compute Unified Device Architecture (CUDA)” with graphics cards that would render them compatible with this technology. NVDIA also formulated Tensor Cores which are specific microprocessors on their graphics cards that would aid in AI models and machine learning. This would ultimately be utilized for creating graphics cards fluent not only for graphics processing but for machine learning and other intensive AI models as well (Khan, Pasha, & Masud, 2021).

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **CPU** | | | **GPU** | | |
| **Processors** | **Minimum Cores** | **Maximum Cores** | **Processors** | **Tensor Cores** | **CUDA Cores** |
| Intel i7, 10th Gen | 4 | 8 | NVIDIA RTX 2080 | N/A | 4352 |
| AMD Ryzen | 4 | 16 |
| Intel Core i9, 10th Gen | 8 | 28 | NVIDIA V100 | 640 | 5120 |
| Intel Xeon Plat. I Gen | 4 | 28 |
| Intel Xeon Plat. II Gen | 4 | 56 | NVIDIA A100 | 432 | 6912 |
| AMD Ryzen Threadripper | 24 | 64 |

Figure 1.1: CPU vs GPU Cores (Khan, Pasha, & Masud, 2021)

The figure presents the core counts of modern CPU vs modern GPUs. It presents how compatible GPUs are to machine learning and AI especially with the integration of specific microprocessors that handle AI model execution and deep learning. It can be observed that compared to the number of cores of a processor, GPUs are exponentially more capable on handling AI related processes.

1. **SECURITY FEATURES ON CHIP**

Microprocessor security is critical in modern computing since processors are the foundation of all digital systems. As technology advances, the dangers and risks to these systems become increasingly complicated. Protecting the integrity and confidentiality of data handled by microprocessors has become a vital issue. Security is no longer only a software concern; it must be integrated into the hardware itself to which numerous microprocessor companies have long developed.

The history of security features embedded in microprocessors is rooted in the need to address hardware-level vulnerabilities that traditional software-based defenses could not mitigate during the development of the Intel 4004 processor. Early computing systems relied primarily on operating system–level access controls (user mode and kernel mode) and security application software, but flaws such as memory leaks and privilege escalation still posed a threat for computer security (Stallings, 2018). To counter these threats, companies introduced hardware-assisted security primitives, including hardware random number generators (RNGs), memory protection units (MPUs), and encryption of instruction sets, such as Intel’s AES-NI for accelerating encryption (Gueron, 2010). By the late 1990s and early 2000s, the notion of a hardware root of trust and isolated execution environments emerged, giving rise to technologies such as Intel Trusted Execution Technology (TXT) which acts similarly to today’s secure boot. It is an embedded hardware technology on intel microprocessors that provides mechanisms for protected execution of malicious instructions and software-based exploits (Intel Corporation, 2024).

Modern microprocessors now implement a wide range of embedded security features. Trusted Platform Module (TPM) 2.0 is a hardware-based security microprocessor feature which securely stores encryption keys, certificates, and platform measurements for identifying valid and licensed software and operating systems in order to deemed fit to operate (Trusted Computing Group, 2019). Similarly, Secure Boot also does the same function (UEFI Forum, 2019). These mechanisms are now embedded in modern microprocessors in order to prevent kernel-level or even hardware level exploits.

1. **INTEGRATION OF CONNECTIVITY ON MICROPROCESSORS AND CHIPS**

The integration of connectivity into microprocessors and microcontrollers has become a defining trend in modern computing. As devices evolve, connectivity allows them to communicate, share data, and interact with larger networks. This shift has enabled the rise of the Internet of Things (IoT), smart devices, and real-time communication systems across industries. By embedding connectivity directly into microprocessors, manufacturers reduce hardware complexity and power consumption which leads to the simplification of microcomputer developments and significant reduction of costs in formulating separate hardware for connectivity.

The history of connectivity in microprocessors and microcontrollers traces back to the mid-1990s, when embedded systems began transitioning from isolated controllers with not concept of connectivity in mind to networked devices. Early efforts included wired communication standards such as Ethernet, which provided links for industrial and enterprise systems (Wired, 1997). By the late 1990s, wireless technologies like Wi-Fi and Bluetooth emerged, marking the first steps toward low-power, short-range connectivity on microcomputers (GSMArena, 2016).

Today, many microcontrollers and microprocessors already come with built-in wireless features. Popular chips like Espressif’s ESP32 include Wi-Fi and Bluetooth, making them widely used in IoT projects (Espressif Systems, n.d.). Other companies such as NXP, also produce chips that support multiple standards like Wi-Fi and Bluetooth (NXP Semiconductors, 2022). Modern designs now focus on making connections more secure, reliable, and energy-efficient.

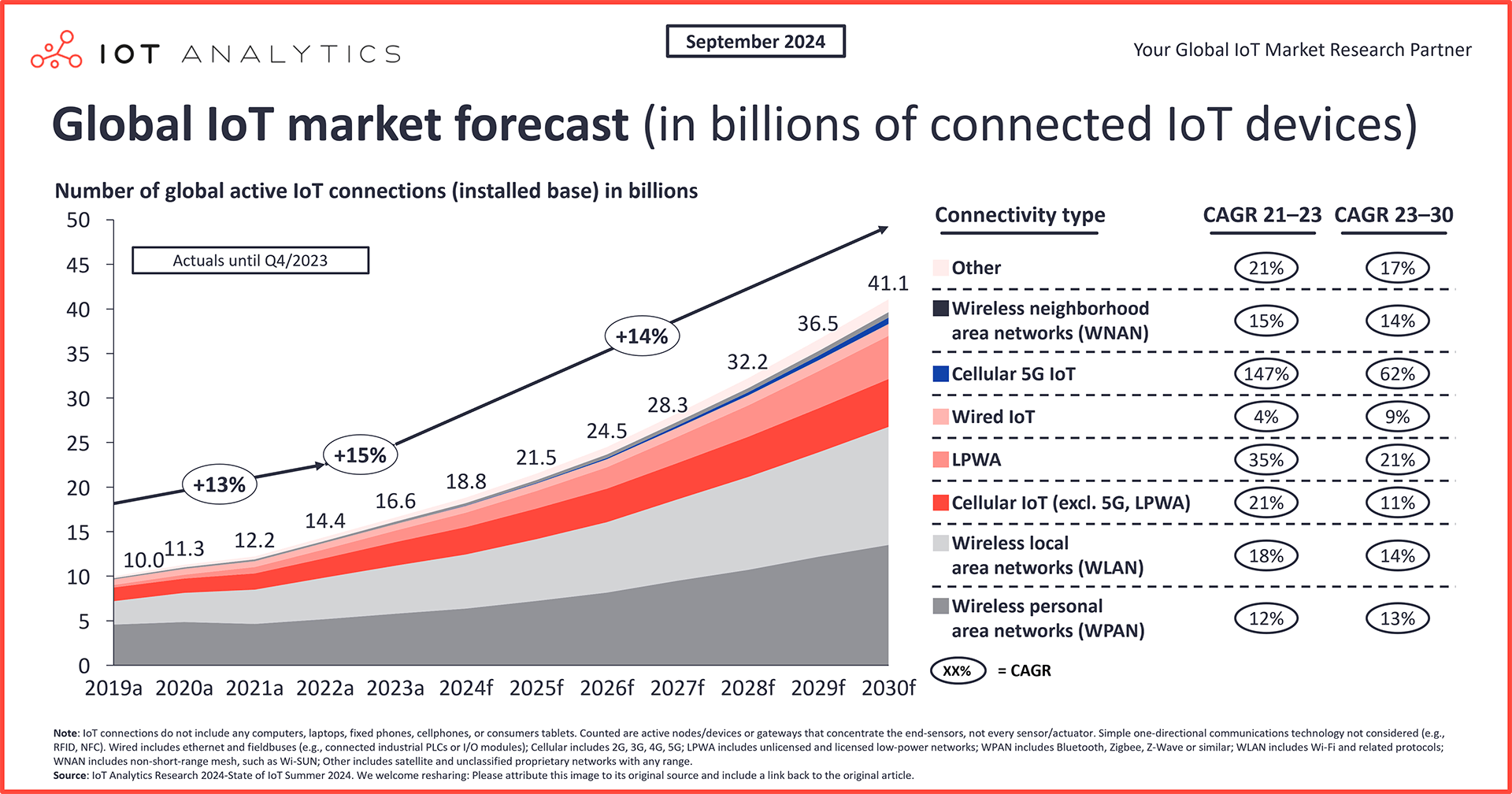


Figure 1.2: Global IoT Market Forecast (Sinha, 2023)

The following graph presents an upward trend of IoT devices utilized during the years 2019 onwards with an expected 14% increase in trend of IoT devices for the years consecutive to 2023. This goes to show that there would be a potential upward trend for more development of microprocessors as and microcomputers with integrated connectivity without the utilization of external hardware just for that purpose.

1. **QUANTUM COMPUTING**

Quantum computing uses the principles of quantum mechanics such as superposition and entanglement in order to process information in ways impossible for classical computers. Unlike traditional bits, “qubits” can hold multiple states at once, allowing faster solutions for complex problems in fields like cryptography, AI, and deep learning (TechRadar, 2025). Although the technology is still in it’s early stages, quantum computing is a realm of computer engineering that would soon come to light as more advances develop.

Quantum computing was first theorized in the 1980s by Richard Feynman and Yuri Manin. The two stipulated that classical systems (such as desktops) cannot outperform quantum systems. This paved the way for the formal definition of quantum computers. In the 1990s, **Shor’s algorithm** showed that quantum computers could factor large numbers exponentially faster. This presented one of the first theoretical results of the prowess of quantum computing. The advances in physical qubit implementations (e.g., superconducting qubits) paved the way for real prototypes. For context, Qubits, with respect to quantum computing, is a type of bit that has three states, 1, 0, and the state in between 1 and 0 (Schneider & Smalley, n.d.). A major milestone occurred in 2019, when Google demonstrated quantum supremacy by solving a problem in 200 seconds that would take supercomputers thousands of years (NIST, 2025).

In 2025, Microsoft introduced the Majorana 1 chip, which uses a new material called a “topoconductor” to create more reliable qubits. For context, Qubits are inherently fragile. Microsoft’s approach uses Majorana zero modes, which acts as foundations for the aforementioned qubits, making the qubit less likely to break down from noise or temperature changes (Koetsier, 2025). This methodology is called “topological protection” which greatly stabilizes the utilization of numerous qubits and reduce errors during vast computations and intensive data-handling.

A graph showing the growth of a company

AI-generated content may be incorrect.

Figure 1.3: Quantum Computing Forecasted Growth (Bobier et al., 2024)

Figure 1.3 presents the forecasted growth of investments towards quantum computing development and market in general. The bar graph shows an inherent trend for quantum computing investment from the years 2019-2024. Projected investment potentials for the industry are expected to be 25% for the proceeding years. This incentivizes companies for further research and development for quantum computing technology for microprocessors that would hopefully reach practical use and be sold commercially.

1. **NEUMORPHIC COMPUTING**

Neuromorphic computing is a new trend in microprocessor design that attempts to copy how the human brain works. Instead of processing data step by step like normal CPUs, these systems use brain-inspired structures to make decisions efficiently. This makes them useful for tasks like pattern recognition, sensory processing, and AI learning.

The concept of neuromorphic computing was first introduced in the 1980s by Carver Mead, who suggested building circuits that mimic biological neurons of a living creature (Mead, 1990). Over time, advances in semiconductor technology made it possible to design processors that use spikes and event-driven signals, similar to how the brain works.

Some of today’s leading neuromorphic processors include Intel’s Loihi chip, which uses “neural networks” to simulate brain-like communication, and IBM’s TrueNorth, which integrates over one million “neurons” on a single chip. These processors are designed to handle real-time learning and adaptive control (Davies et al., 2018). Neuromorphic computing is still in its early stages but shows strong potential for future AI models.

A graph of the market size

AI-generated content may be incorrect.

Figure 1.4: Neuromorphic Computing Market Projection (Precedence Research, 2025)

The following bar graph presents projection rates for Neumorphic Computing. 2024-2025 shows an increase in Nuemorphic computing. For the consecutive years, there is a projected upward trend up until 2034 for Nuemorphic computing investment. This stipulates that there would be yearly significant developments with regards to this specific microprocessor industry.

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